CLAIMS

What is claimed is:

1. A system comprising:

a) an array of photocells that are arranged in rows and columns; and

b) a sequential readout circuit that is coupled to one column of the array at a time and that processes one photocell at a time.

2. The system of claim 1

wherein the sequential readout circuit sequentially reads out the value of the photocells one photocell at a time.

3. The system of claim 1

wherein the sequential readout circuit determines a difference between a final integration light value and a reset value for each photocell in a time sequential manner.

4. The system of claim 1 wherein the array includes a plurality of columns; wherein the system further includes

a sample and hold circuit for each column; wherein each sample and hold circuit samples and holds the voltage value of a photocell that is disposed in the respective column.

5. The system of claim 1 wherein the sequential readout circuit includes

an amplifier that includes

a first input;

an output; and

an integration capacitor having a first electrode for coupling to the first input and a second electrode for coupling to the output of the amplifier;

wherein the amplifier includes a charge transfer mode and a unity gain mode.

6. The system of claim 1 wherein the sequential readout circuit includes a level shifting circuit coupled to the first input and the output of the amplifier for performing level shifting of the output of the amplifier.

7. The system of claim 1 wherein the sequential readout circuit includes a gain manipulation circuit coupled to the first input and the output of the amplifier for performing gain manipulation of the amplifier.

8. The system of claim 1 wherein each photocell includes

a photodiode for detecting light and responsive thereto for generating a voltage representation thereof; wherein the photodiode includes an integration node;

a first transistor coupled to the photodiode for resetting the integration node in response to a reset signal;

a second transistor coupled to the integration node for shifting the level of the voltage at the integration node; and

a third transistor coupled to the second transistor for reading out the level-shifted voltage in response to a read signal.

9. The system of claim 1 wherein the system is implemented in one of a scanner application, an optical mouse application, a video game controller application, a movement encoder application, a near field application, and a far field application.

10. A sequential readout circuit for coupling to an array of photocells; wherein the array includes at least a first row, a first column, a second column, a first

photocell that is disposed in the first row and the first column, and a second photocell that is disposed in the first row and in the second column, the sequential readout circuit comprising:

a) an amplifier for reading out the value of the photocells in the array one photocell at a time;

b) a first switch for selectively coupling the amplifier to the first column; and

c) a second switch for selectively coupling the amplifier to the second column.

11. The sequential readout circuit of claim 10

wherein the single amplifier determines the difference between a reset voltage (V_{reset}) and a light voltage (V_{light}) for the first photocell and the second photocell in a time sequential manner.

12. The sequential readout circuit of claim 10 further comprising:

a sample and hold circuit for each column; wherein each sample and hold circuit samples and holds the voltage value of a photocell that is disposed in the respective column.

13. The sequential readout circuit of claim 12 wherein each sample and hold circuit includes

a capacitor, and

a transistor coupled to the first sampling capacitor.

14. The sequential readout circuit of claim 10

wherein the amplifier includes a charge transfer mode, a unity gain mode, a first input; and an output; and